Hardware ODE Solvers Using Stochastic Circuits

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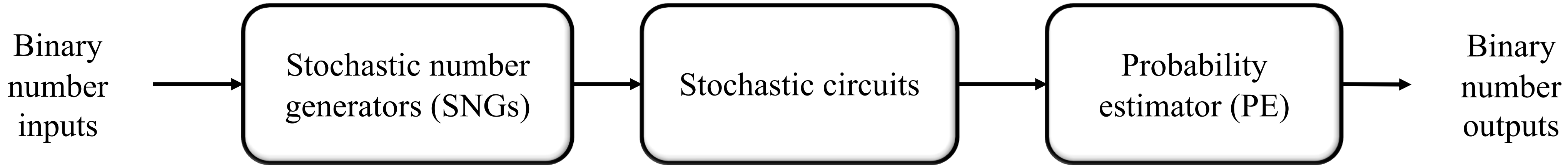
Outline

- ❑ **Introduction to stochastic computing**
  - Stochastic integrators
- ❑ **Formulation of stochastic integrators**
- ❑ **Proposed stochastic ODE solver design**
  - Nonhomogeneous ODEs
  - Systems of ODEs
  - Higher-order ODEs
- ❑ **Error assessment and error reduction schemes**
- ❑ **Hardware evaluation and performance comparison**
- ❑ **Conclusion and future work**

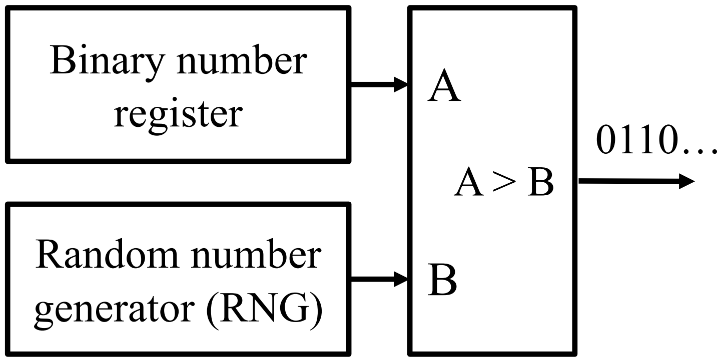
Introduction

- In stochastic computing (SC), information is encoded and processed by random binary bit streams.

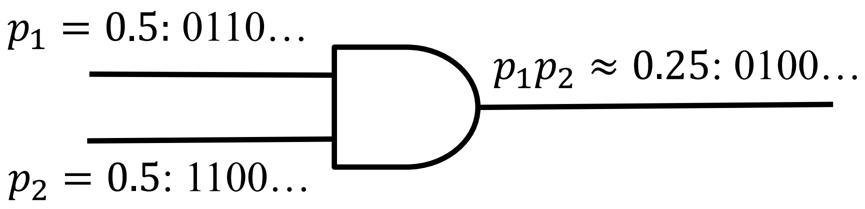


A stochastic computing system

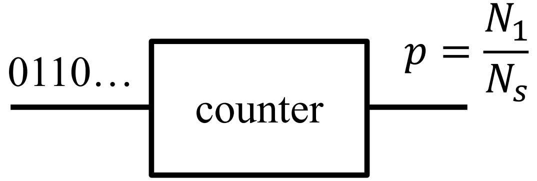
N_1: number of 1's in the stochastic sequence
N_S: bit length of the stochastic sequence



An SNG



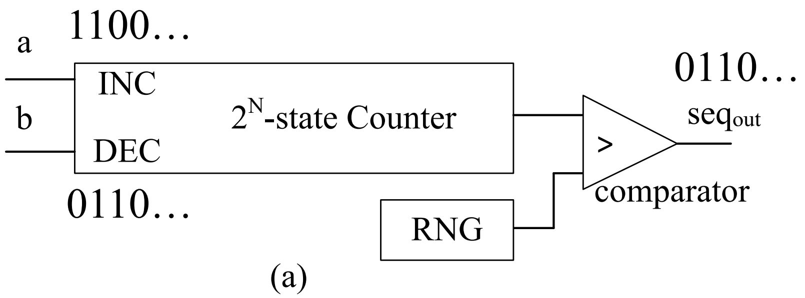
A unipolar stochastic multiplier



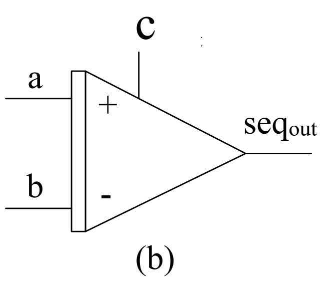
A PE

[Gaines 1969]

Stochastic Integrator



A stochastic integrator



Symbol

$$c_{i+1} = \begin{cases} c_i + 1/2^N & a_i = 1 \ \& \ b_i = 0 \\ c_i - 1/2^N & a_i = 0 \ \& \ b_i = 1 \\ c_i & a_i = b_i \end{cases}$$

⇩

$$c_{i+1} = c_i + \frac{1}{2^N}(a_i - b_i). \quad (1)$$

Accumulating (1) for $i = 0, 1, 2, \ldots, k-1$

$$c_k = c_0 + \frac{1}{2^N}\sum_{i=0}^{k-1}(a_i - b_i) \ . \quad (2)$$

Taking the expectation of (2)

$$\mathbb{E}[c_k] = c_0 + \frac{1}{2^N}\sum_{i=0}^{k-1}(\mathbb{E}[a_i] - \mathbb{E}[b_i]). \quad (3)$$

Function of a stochastic integrator: $seq_{out} \approx \int (a-b)dt$

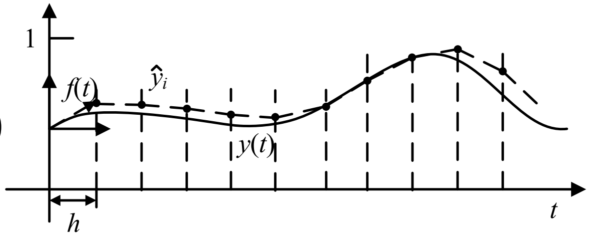
An example of stochastic integrator (N=8)

i	a_i	b_i	c_i	RN$_i$	seq$_{\text{out}}$
0	1	0	$(0.10000000)_2$	0.75	0
1	1	1	$(0.10000001)_2$	0.20	1
2	0	1	$(0.10000001)_2$	0.19	1
3	0	0	$(0.10000000)_2$	0.62	0
……					

[Saraf et al., DATE 2014]

Unbiased Euler Solution Estimator

Euler Method: $\frac{dy(t)}{dt} = f(t)$



$$\hat{y}_{i+1} = y_i + hf(t_i)\,, \qquad (4)$$

where h is the step size and $t_i = h \cdot i$.

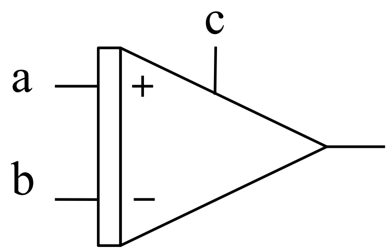
(4) can be changed to:

$$\hat{y}_{i+1} = y_i + hf(hi) \approx y(h(i+1)). \qquad (5)$$

By accumulating (5) for $i = 0, 1, 2, \ldots, k$

$$\hat{y}_k = y_0 + h\sum_{i=0}^{k-1} f(hi) \approx y(hk). \qquad (6)$$

Stochastic Integrator:



$$\mathbb{E}[c_k] = c_0 + \frac{1}{2^N}\sum_{i=0}^{k-1}(\mathbb{E}[a_i] - \mathbb{E}[b_i]). \qquad (3)$$

Let $c_0 = y_0, \mathbb{E}[a_i] - \mathbb{E}[b_i] = f(hi)$, then

$\mathbb{E}[c_k] = \hat{y}_k \approx y(\frac{k}{2^N})$, with $h = \frac{1}{2^N}$.

A stochastic integrator provides an unbiased estimate to the Euler solution with a step size of $1/2^N$.

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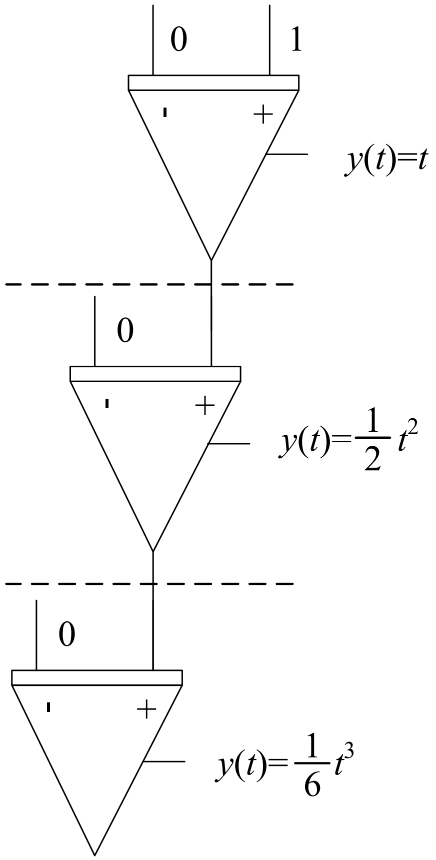
Stochastic Solvers for Nonhomogeneous ODEs



$(\mathbb{E}[a_i - b_i] = f(t) = 1)$

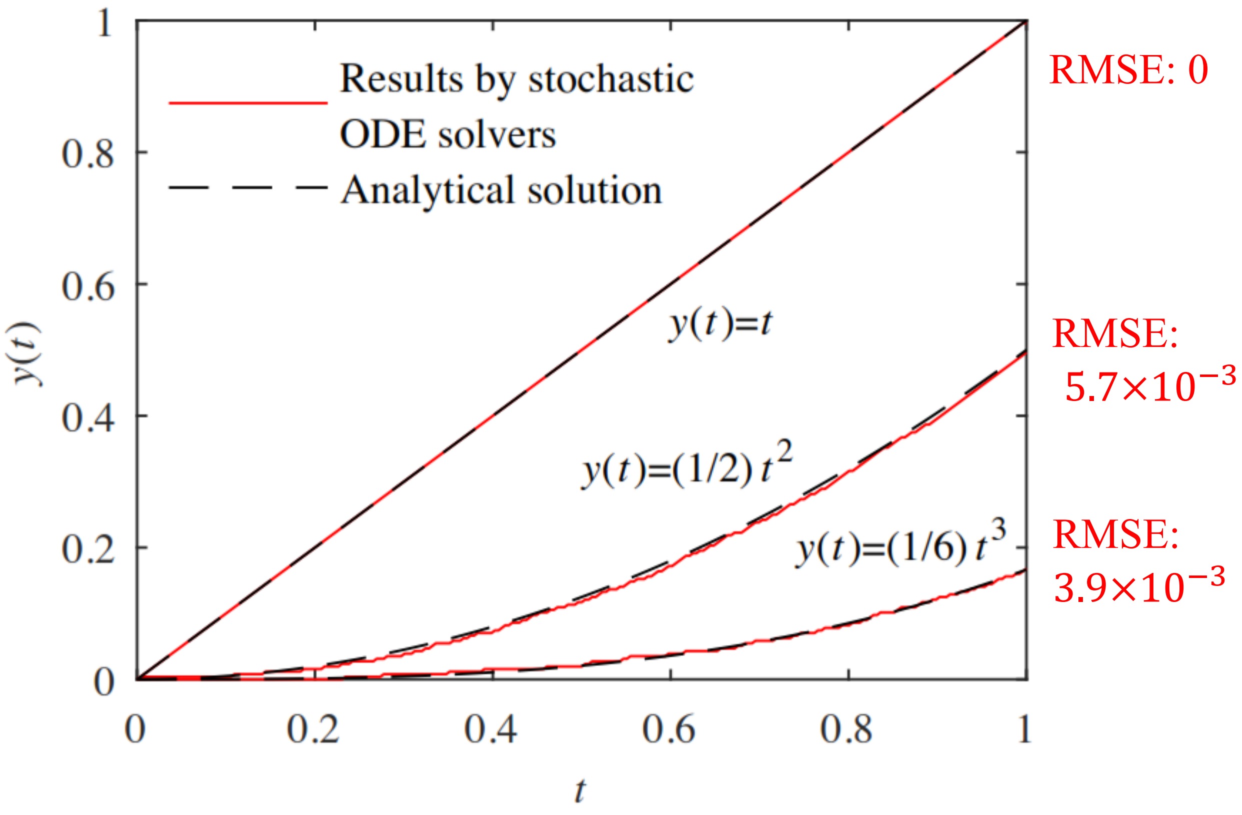
$$\frac{dy(t)}{dt} = 1 - 0 \qquad (7)$$

$(\mathbb{E}[a_i - b_i] = f(hi) = hi)$

$$\frac{dy(t)}{dt} = t \qquad (8)$$

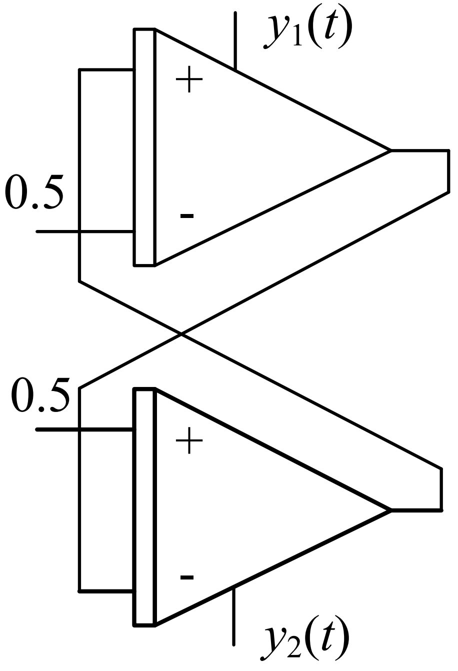
$$\frac{dy(t)}{dt} = \frac{1}{2}t^2 \qquad (9)$$

A stochastic ODE solver for (7), (8) and (9).



Hardware solution produced by stochastic ODE solver vs. analytical solution.

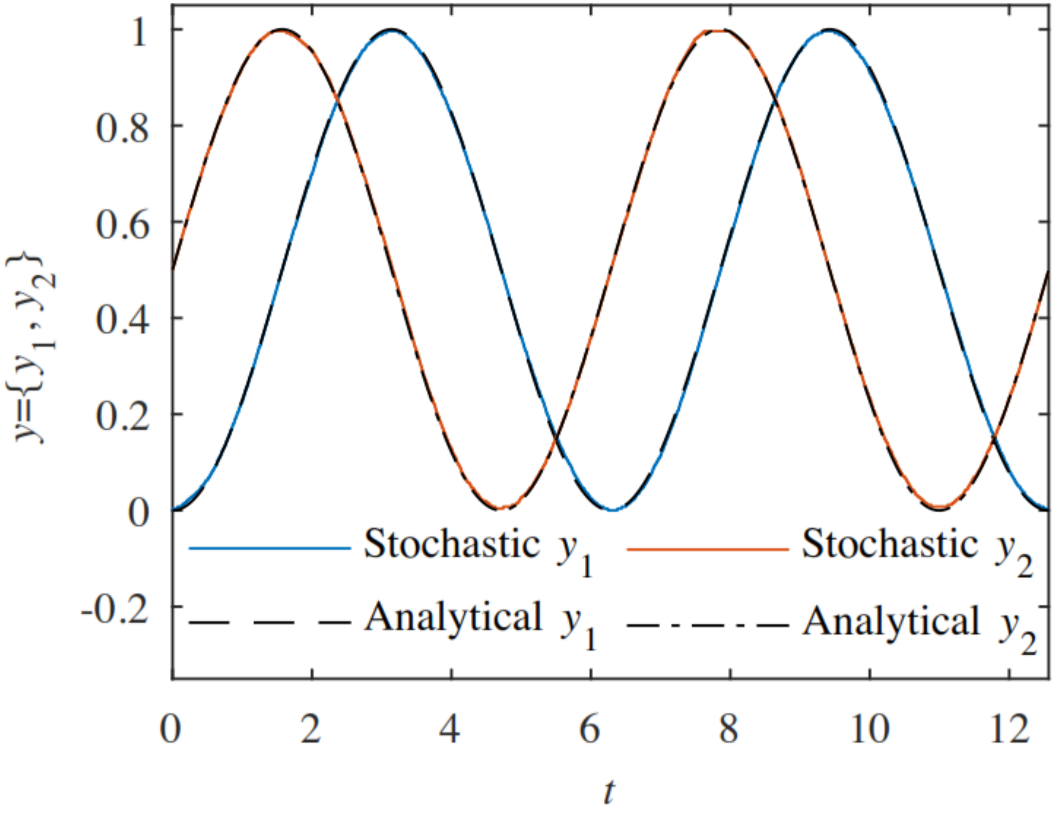
Stochastic Solvers for Systems of ODEs



$$\begin{cases} \frac{dy_1(t)}{dt} = y_2(t) - 0.5 \\ \frac{dy_2(t)}{dt} = 0.5 - y_1(t) \end{cases} \quad (10)$$

A stochastic ODE solver for (10).

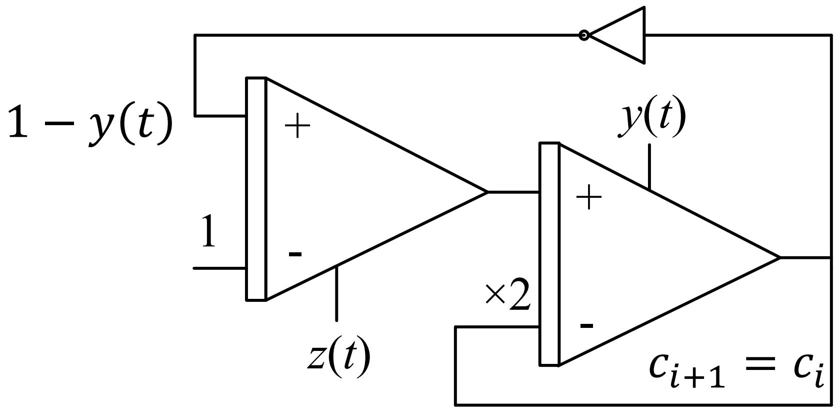
RMSE: 4.7×10^{-3}



Hardware solution produced by stochastic ODE solver vs. analytical solution.

Higher-order Stochastic ODE Solvers

$$\frac{d^2y(t)}{dt} + \frac{2dy(t)}{dt} + y(t) = 0 \qquad (11)$$

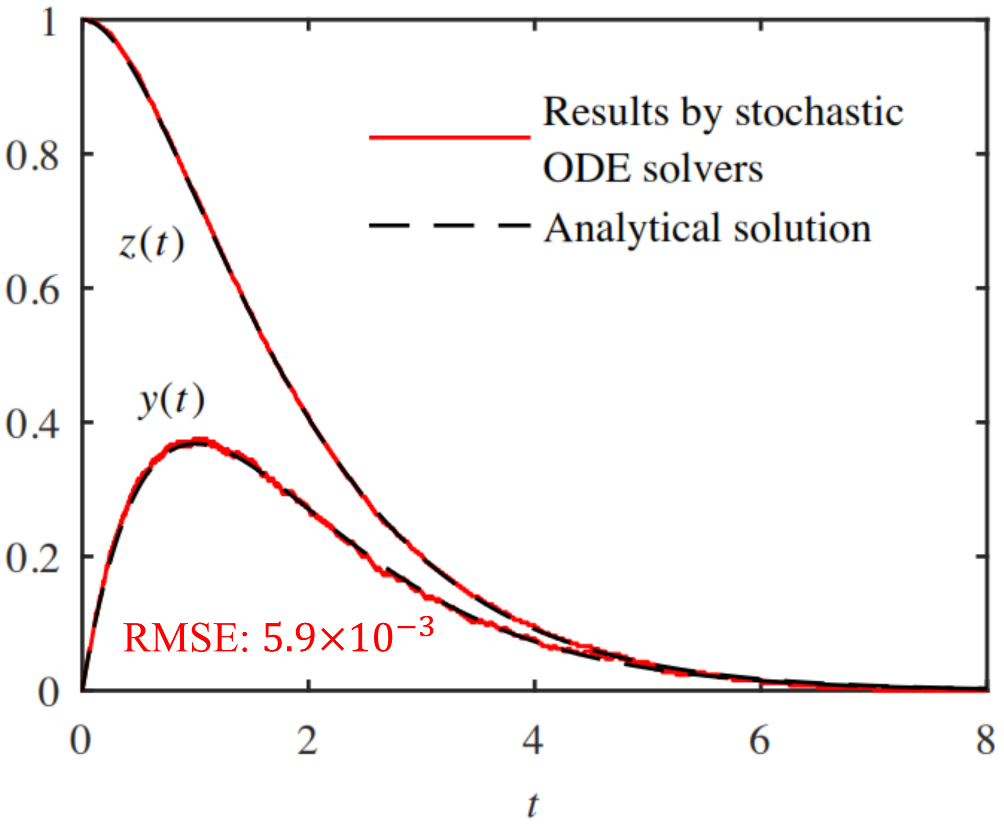


$$c_{i+1} = c_i + \frac{1}{2^N}(a_i - 2b_i)$$

$$\frac{dz(t)}{dt} = -y(t) \qquad \frac{dy(t)}{dt} = z(t) - 2y(t)$$

Introduce an auxiliary function z(t), satisfying

$\frac{dz(t)}{dt} = \frac{d^2y(t)}{dt} + \frac{2dy(t)}{dt}$, to reduce the order.



Hardware solution produced by stochastic ODE solver vs. analytical solution.

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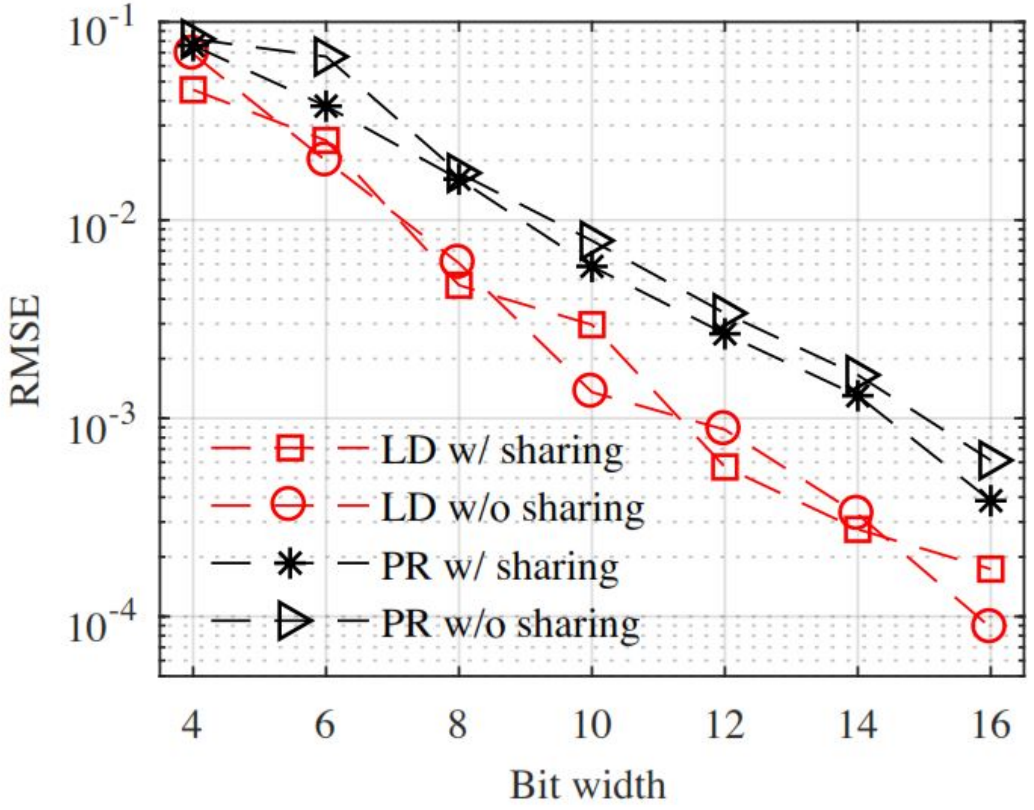
Error Assessment of a Stochastic Integrator

$$\mathbb{E}[c_k] = c_0 + \frac{1}{2^N}\sum_{i=0}^{k-1}\mathbb{E}[(a_i - b_i)] \;= \hat{y}_k \approx y(\frac{k}{2^N}).$$

- **Error of Euler method**
  - Reduced by using a smaller step size, i.e., increase the size of counter *N*.
- **Random fluctuation of stochastic circuits**
  - The use of low-discrepancy (LD) sequences can reduce random fluctuation.
  - Sharing RNGs for generating the inputs of the stochastic integrator can also reduce the variance.



*PR: pseudorandom sequences generated by the linear feedback shift registers (LFSRs).

[Alghi and Hayes, DATE 2014]

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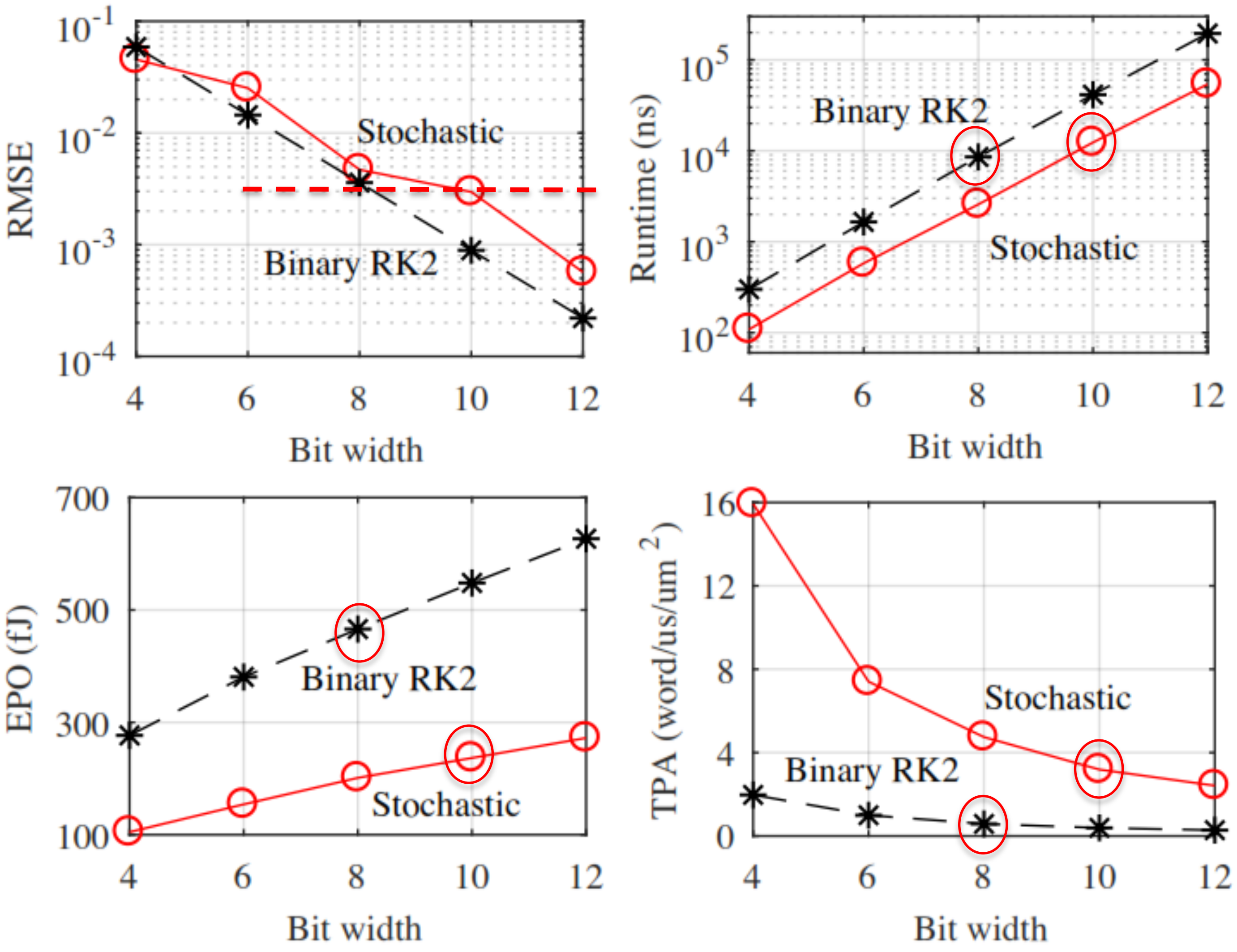
Hardware Evaluation and Performance Comparison

ODE	Metric	SC	Binary*	Improvement
(8)	Energy/Operation (fJ)	144.49	201.05	28%
	Throughput/Area (solution/$\mu s/\mu m^2$)	13.84	3.86	258%
	Minimum runtime (ns)	104.96	263.68	60%
(9)	Energy/Operation (fJ)	186.10	253.05	26%
	Throughput/Area (solution/$\mu s/\mu m^2$)	9.76	0.94	934%
	Minimum runtime (ns)	104.96	586.24	82%
(10)	Energy/Operation (fJ)	201.21	466.00	56%
	Throughput/Area (solution/$\mu s/\mu m^2$)	4.75	0.58	716%
	Minimum runtime (ns)	2573.59	8557.20	70%
(11)	Energy/Operation (fJ)	156.04	591.62	**74%**
	Throughput/Area (solution/$\mu s/\mu m^2$)	5.68	0.44	**1184%**
	Minimum runtime (ns)	1597.44	6819.84	**76%**

*Binary circuits are built by shifters and adders to save hardware cost. The algorithm implemented by binary circuits are the 2nd Runge-Kutta method with 8-bit width. The stochastic circuits are also 8-bit width.

Stochastic vs. Binary Circuits with Different Bit Widths



Comparison of stochastic and binary ODE solvers with different bit widths.
For stochastic ODE solvers, it is the bit width of counter.

Stochastic circuits with 10-bit counters vs. 8-bit binary circuits

Advantages:

- ❑ **Energy per operation**
- ❑ **Throughput per area**
- ❑ Slightly better accuracy

Disadvantage:

- ❑ Slightly longer runtime

EPO: Energy per operation
TPA: Throughput per area

Conclusion and Future Work

- A novel design for solving an ODE is proposed by using a stochastic integrator to implement the accumulation in the Euler numerical method.
- The stochastic integrator provides unbiased estimate of the Euler numerical solution.
- The stochastic ODE solver has a lower energy consumption, higher TPA and shorter minimum runtime compared to binary designs.
- The error analysis shows that the sharing of RNGs is effective in reducing error for pseudorandom sequences, while it is less effective for LD sequences.
- Extended range of representation for the solutions will be investigated in the future work.

References

- B. R. Gaines. 1969. Stochastic Computing Systems. Springer US, 37–172.
- J. C. Butcher. 1987. The Numerical Analysis of Ordinary Differential Equations: Runge-Kutta and General Linear Methods. Wiley-Interscience.
- N. Saraf, K. Bazargan, D. J. Lilja, and M. D. Riedel. 2014. IIR Filters using Stochastic Arithmetic. In DATE.
- B. R. Land. 2006. DDA on FPGA. http://people.ece.cornell.edu/land/courses/ece5760/DDA/index.htm. Accessed: 2016-10-12.
- J. P. Hayes. 2015. Introduction to Stochastic Computing and Its Challenges. In DAC.
- M. Gerber and N. Chopin. 2015. Sequential Quasi Monte Carlo. Journal of the Royal Statistical Society: Series B (Statistical Methodology) 77, 3, 509–579.
- S. Liu and J. Han. 2017. Energy Efficient Stochastic Computing with Sobol Sequences. In DATE.
- Y. Liu and K. K. Parhi. 2016. Computing Complex Functions Using Factorization in Unipolar Stochastic Logic. In GLSVLSI.

Thank you for your attention.